REMARKS

Claim 5 is edited without narrowing that could invoke Festo-like limitations.

The editing confirms that the claimed bootstrap circuit (the current generation circuit 124 in the specification) increases the input impedance of the output circuit 23 as described in the Response of October 11, 2005, and reduces shock noise as described at page 7, lines 15-17, of the specification.

In relation to the rejection of claims 5 - 9 under 35 USC 102 for anticipation by the newly cited Berringer, et al. patent, however, attention is directed to increasing with the bootstrap circuit input impedance of the output circuit that generates a supply voltage for a load from a delay-circuit delayed input voltage, because this locates the bootstrap- increased input impedance of the claimed output circuit after the delay circuit. The claimed bootstrap circuit is after the delay circuit on an input side of the output circuit.

In the Berringer, et al. patent, the Action finds a delay circuit 21, 22 in the middle of Fig. 1. The output terminal 41 is on the right for the high-voltage transistor 53 and motor 52, which are the load. Therefore, the output circuit that generates a supply voltage for a load from a delay-circuit delayed input voltage, as claimed, must be on the right in Fig. 1 of the patent, between the delay circuit and the load, neither the output circuit nor the load being identified in the Action which, for that reason also, is insufficient for a rejection.

The bootstrap circuit 15 is on the left of Fig. 1 of the patent, not on the right with an input to an output 41, as claimed, between the delay circuit 21,22 identified in the Action and the output 41 found as above. Therefore, the rejection under 35 USC 102 for anticipation is traversed.

The rejection for anticipation should not be converted into one under 35 USC 103 for obviousness from the patent, because the bootstrap circuit 15 in the Berringer, et al. patent does not function to increase output circuit impedance or reduce shock noise, as claimed, either.

The bootstrap circuit 15 of the patent is not connected to the output circuit on the right of Fig. 1 and, therefore, cannot affect its input impedance. The bootstrap circuit 15 is connected in a circuit 12 between a low-voltage input 38 and current mirror 17 and amplifier 18 leading to the delay circuit 21, 22. As described at column 5, lines 20 - 41, of the patent:

> The bootstrap effect of capacitor 15 causes the value of the motor supply voltage 50 to be added to both sides of capacitor 15.
> .....
> This causes diode 16 to become reversed biased .....
> .....
> Since diode 16 is reversed biased, current required to maintain conduction through high voltage transistor 53 is supplied by capacitor 15.

The bootstrap circuit 15 in the patent is an input current supply and not an output impedance heightener (current reducer) and noise reducer, as claimed.

Resort to Fig. 3 of the application shows further differences. The bootstrap circuit 124 or, more strictly, transistor Q2 is between a current mirror Q3, Q4 and the output circuit 23 that controls an amplifier 12. Fig. 1 of the Berringer, et al. patent shows the current mirror 17 between the amplifier 18 and the bootstrap 15. In short, the claimed invention of Fig. 3 is not obvious from the Berringer, et al. invention of Fig. 1, because they do not even look similar.

Reconsideration and allowance are, therefore, requested.

Respectfully submitted,

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